Using LME49810 to Build a High-Performance Power Amplifier – Part II

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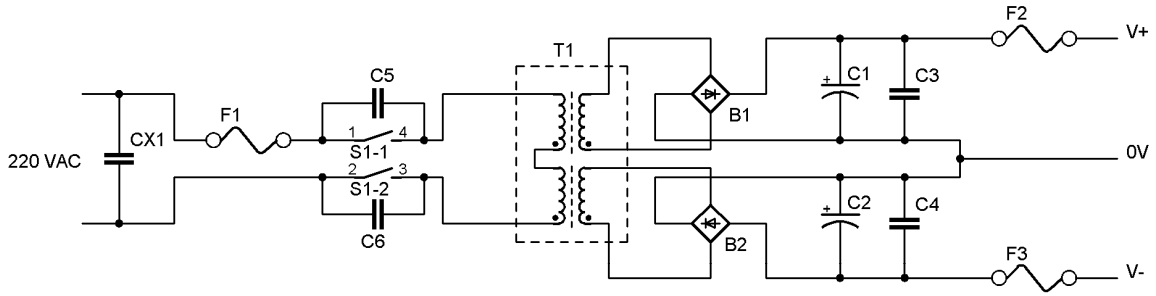
In this report, the power supply and component values are presented. Amplifier bias optimization will be given. The bias pot was adjusted with THD and output spectrum monitored to find an optimum level. Followed are results of performance evaluation of the amplifier including THD, IMD and square wave test.

Power Supply

I selected an unloaded DC voltages equal to +/- 55 V. This insure the output power is at least 120 W for 8 Ω. The power supply schematic is shown in Figure 1. A 0.15 uF X-capacitor is placed across the AC mains input to minimize RF interference. The AC mains input and DC outputs are fuse protected. Fuses placed at the DC rails can cause higher output-signal induced ripple due to their finite resistance. A 5 A fuse was measured by a precision LCR meter. It has 17.43 mΩ resistance at 1 kHz as shown in Figure 2. The resistance increases slightly in higher frequencies due to skin effect. Figure 3 shows the DC rail waveform (scope input AC coupled) under different scenarios. We can see that there is a 1 kHz signal on top of the 100 Hz ripple coming from mains and rectification. The level is increased for the case with fuse used. However, increased ripple level does not seem to affect the amplifier performance. The amplifier has sufficiently high PSRR to suppress such ripple to a diminishing level at its output.



CX1: 0.15 uF X-capacitor
C5, C6: 0.01 uF
C1, C2: 22000 uF, 80 V
C3, C4: 0.1 uF
F1: 5 A slow blow
F2, F3: 5 A
T1, B1, B2: read text

Figure 1 Power supply

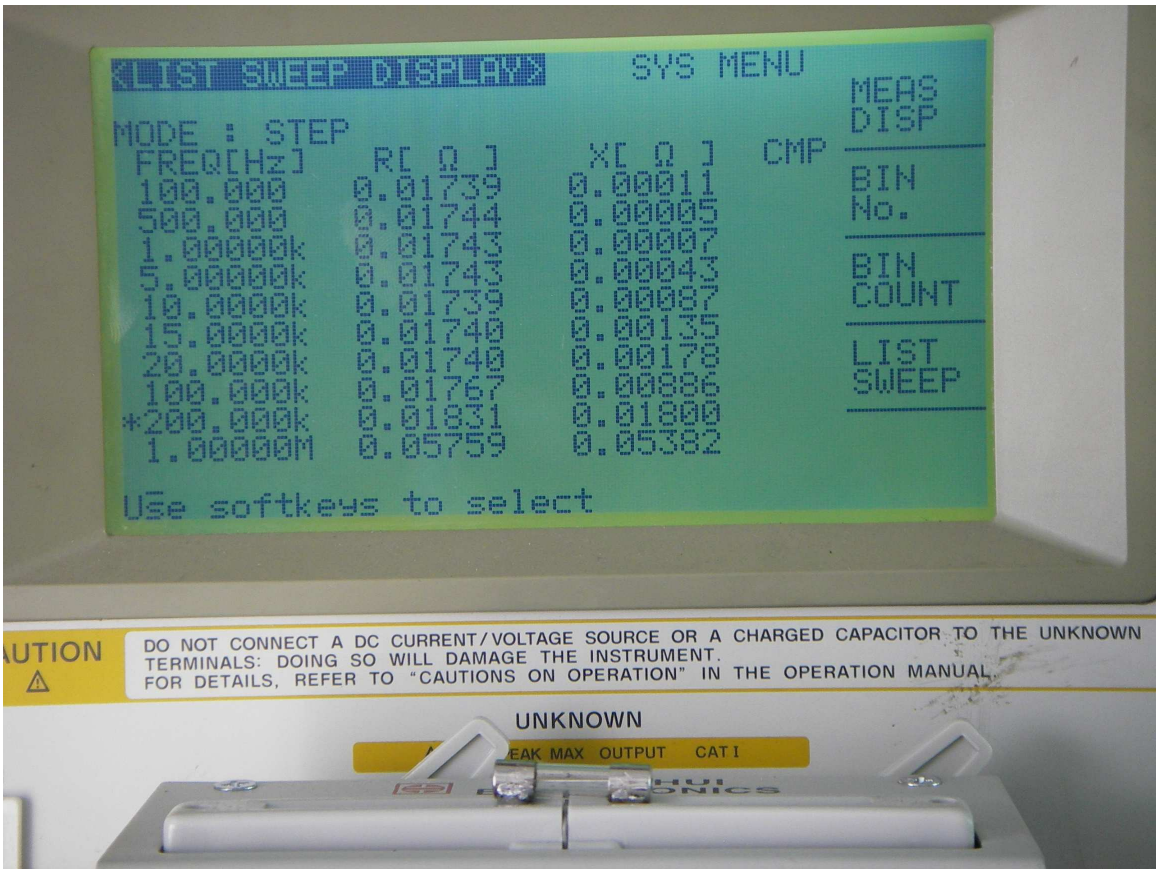


Figure 2 Impedance of a 5 A fuse for various frequencies.

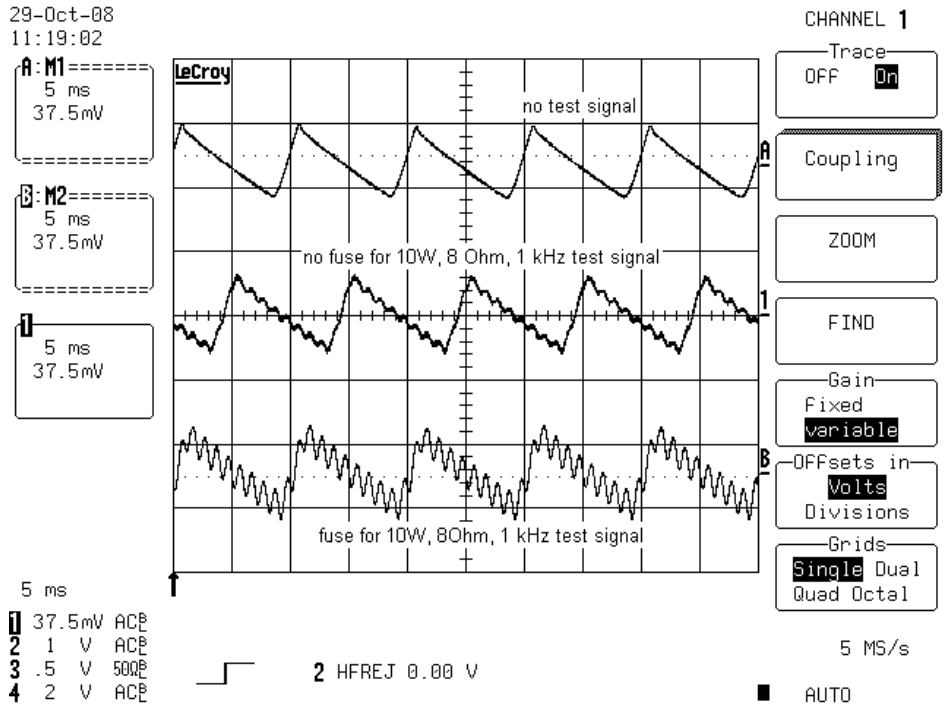


Figure 3 Signal induced ripple on top of 100 Hz ripple of DC rails: Top: no output, middle: 10 W with no fuse used, bottom: 10 W with fuse used.

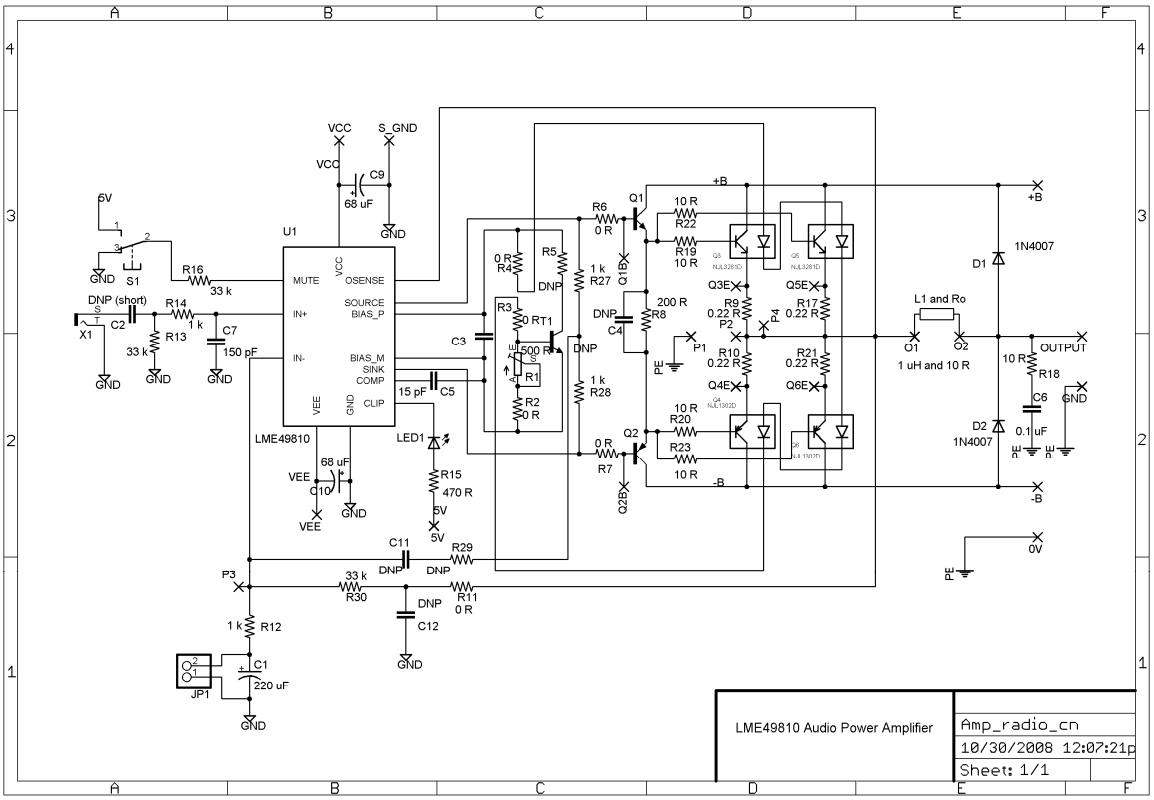


Figure 4 Amplifier schematic with component values.

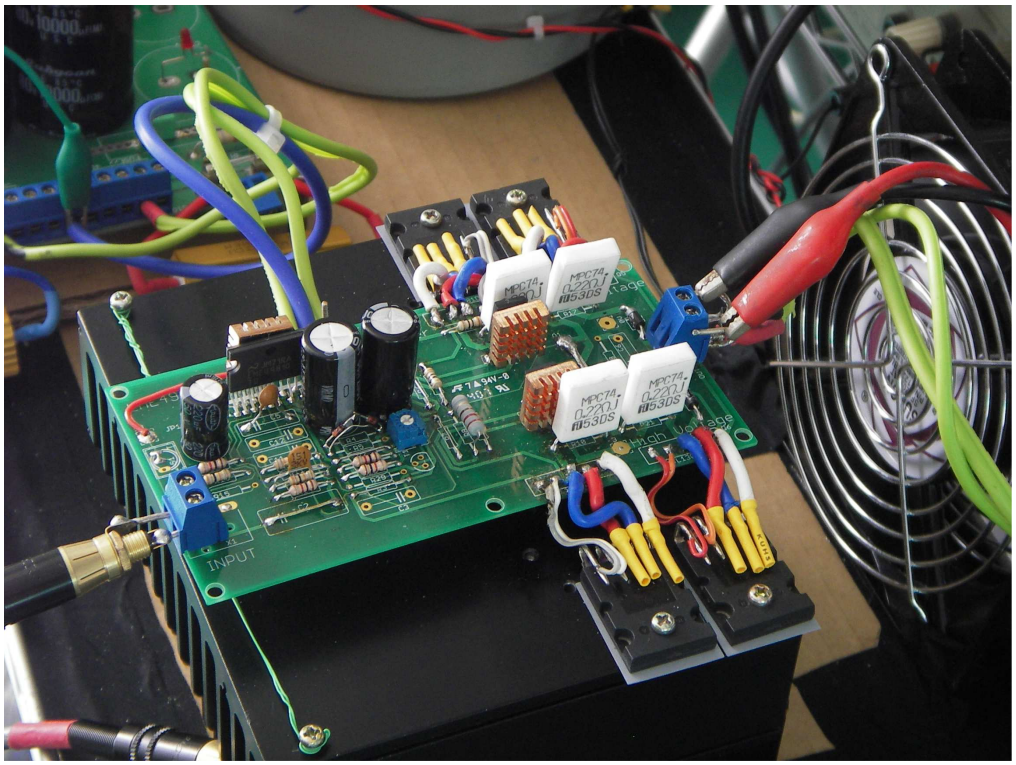


Figure 5 Amplifier under test.

Finding Optimum Bias Level

The assembled amplifier is shown in Figure 5. The output stage of the amplifier will be biased in the so-called Class AB. Bias voltage for driver stage and output devices are generated by the bias pot connected to BiasP and BiasM pins and the diodes inside the output devices. The data sheet of LME49810 mentions that the current from BiasP and BiasM pin is typically 2.8 mA. Suppose all transistors $V_{BE\text{-}on}$ is 0.6V, the pot has to have at least 1.2 V across it to bias driver and output transistors. The theoretical pot resistance is 1.2V/2.8 mA = 428 Ω. A 500 Ω pot is employed in the circuit.

We want to have a bias voltage that is sufficient to turn on all output devices at zero and low level output to avoid crossover distortion. The bias level adjustment was assisted with simultaneously measuring THD+N and FFT analysis of output waveform.

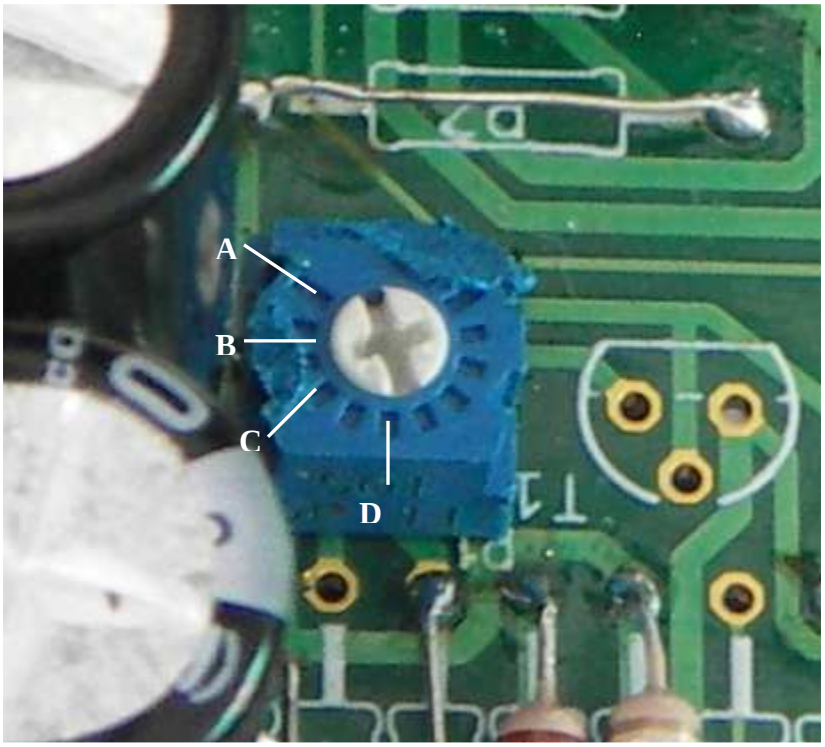


Figure 6 Pot positions for different bias levels.

We adjusted the pot slowly while observing THD+N of a 1 kHz signal with 10 W output to an 8 Ω load. The analyzer's measurement bandwidth was set to 22 Hz to 30 kHz.

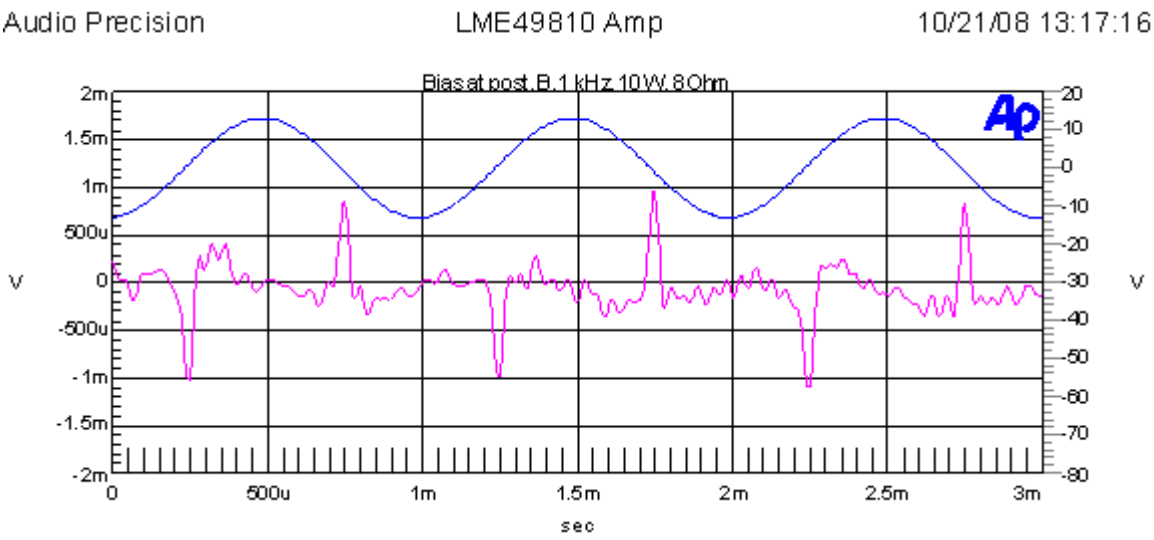


Figure 7 Upper: output waveform, bottom: THD+N residual for bias pot at position B.

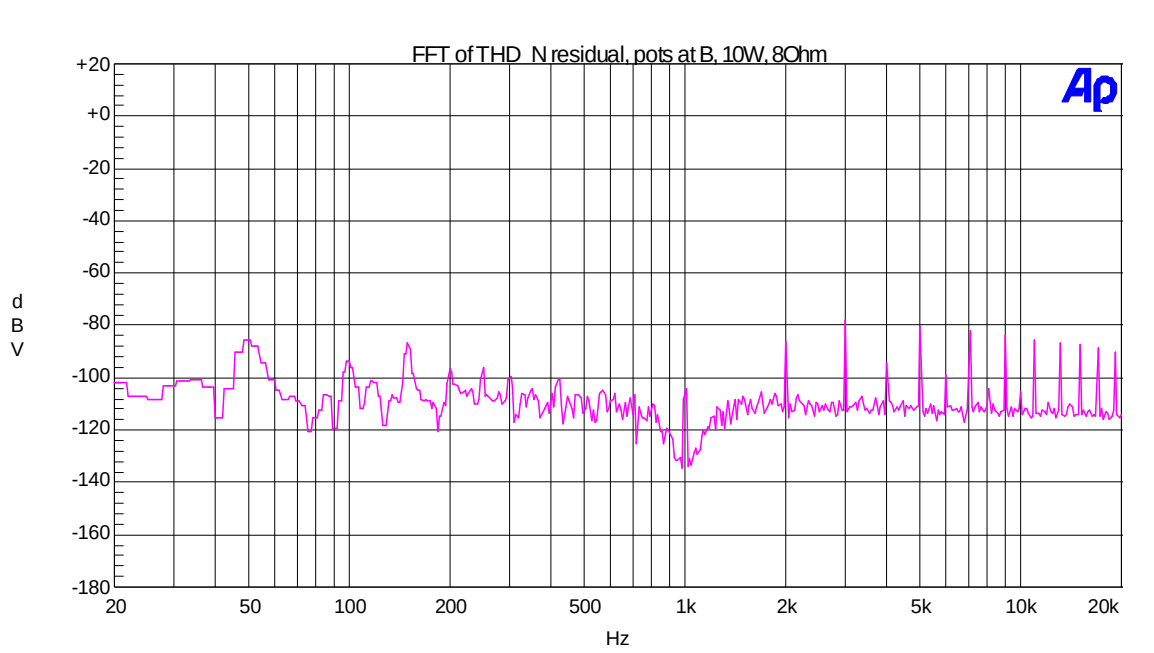


Figure 8 FFT of THD+N residual when bias pot at position B.

When the pot was at position B as shown in Figure 6, THD+N was 0.0056 %. The bias current for each output transistor was about 8 mA. The THD+N residual (signal with fundamental removed) is shown in Figure 7. We can clearly see crossover discontinuities which occur at zero crossings of the output waveform. The FFT of this residual as shown in Figure 8 also reveals rich of harmonics. Nevertheless, their levels are 80 dB down compared to the output level. One may argue that such low level distortion contents are not hearable and we shall stop here. The author believes optimizing the technical specification of a given circuit is fundamental to engineering. How does it affect to sound

quality is a subjective matter beyond the scope of this article. The bias level was increased further to position C. With this bias level (80 mA per output transistor), THD+N decreased to 0.0035 %. The corresponding FFT of the residual is shown in Figure 8. Although the performance is improved, we still can see many some high order harmonics. The bias level was slowly increased again while FFT analysis of residual signal was running. A bias level was eventually reached where harmonics higher than third order vanished as shown in Figure 10. Figure 11 shows the output waveform and residual. It clearly indicates the residual is practically pure third harmonic. The bias pot is now at position D and the THD+N = 0.001 %*.

* The 400 Hz high-pass filter was enabled to remove interference from 100 Hz hum in order to see small amount of differences.

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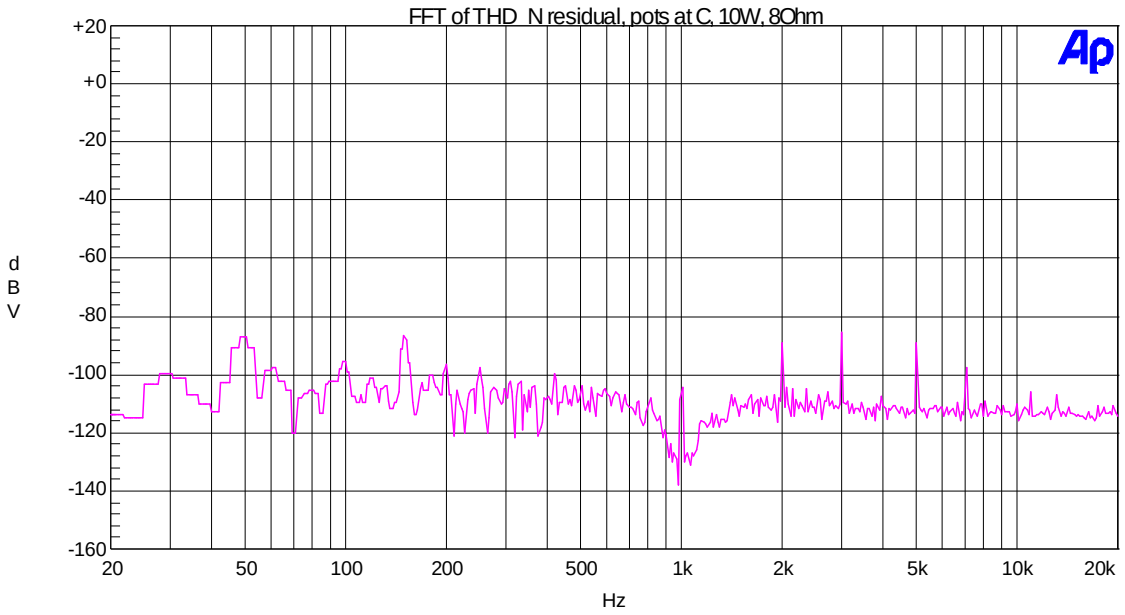

Figure 9 FFT of THD+N residual when bias pot at position C.

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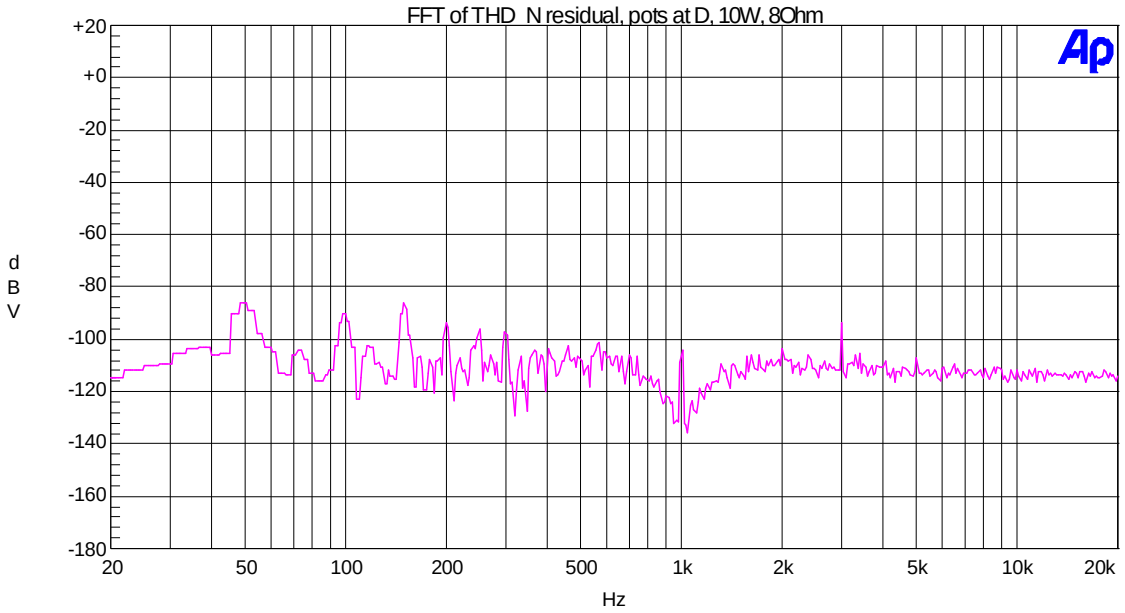

Figure 10 FFT of THD+N when bias pot at position D.

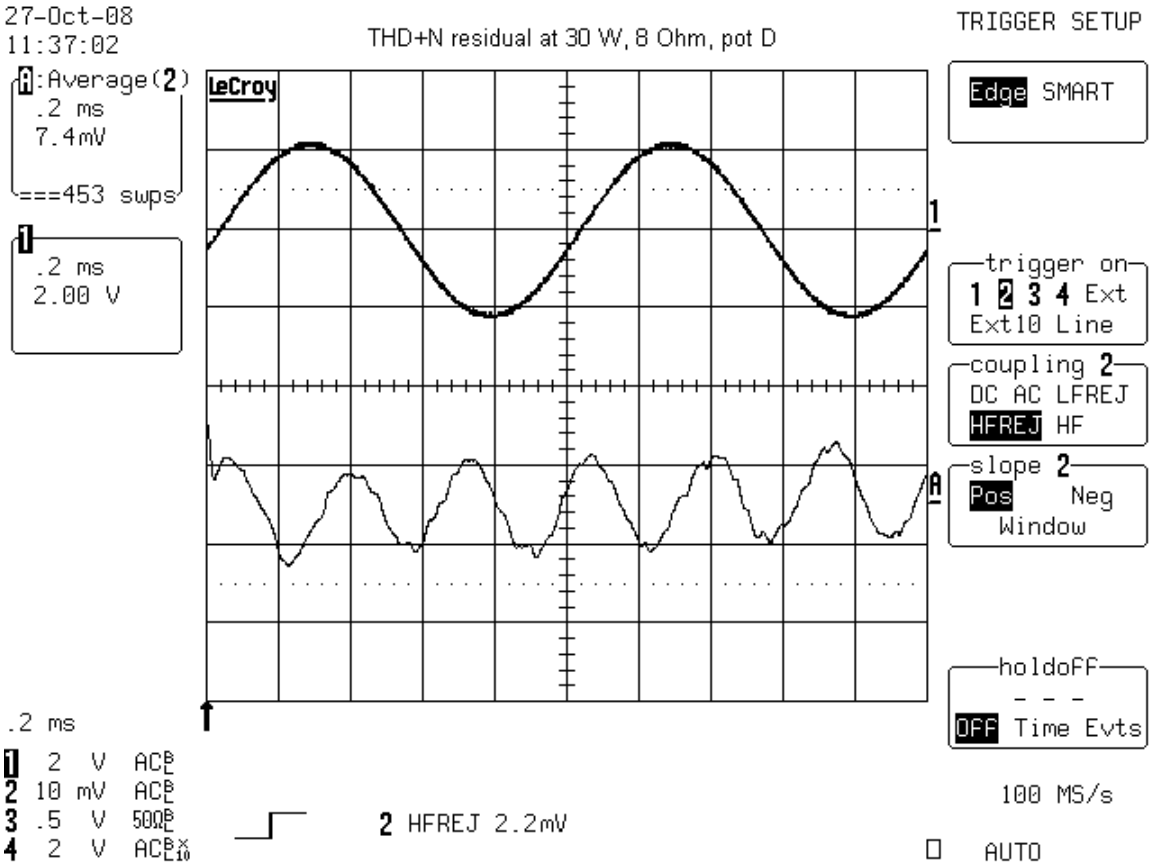

Figure 11 1 kHz, 30 W, 8 Ω. Top: THD+N residual, bottom: output waveform.

THD+N versus output level of the three bias levels (pot position B, C and D) obtained above was evaluated. It is shown in Figure 12. We can see that THD+N of pot at D at high output level is slightly higher than that of pot at C. The quiescent current of pot at D for each output transistor is 400 mA. The heat sink is fairly hot.

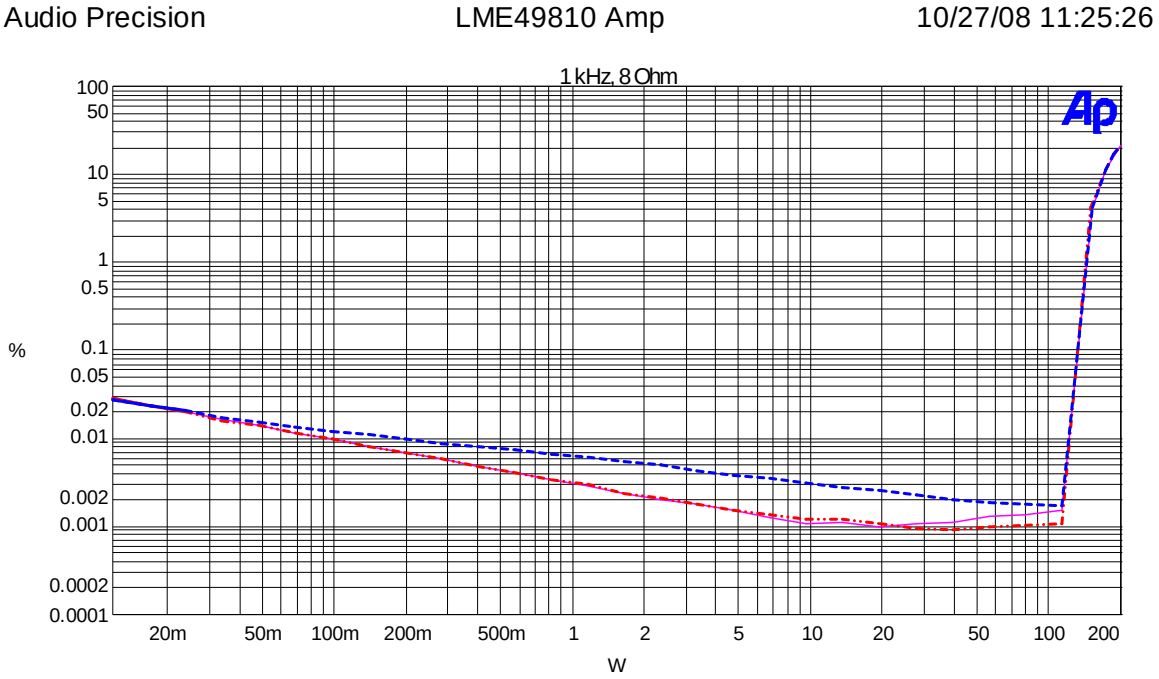

Figure 12 THD+N vs output level (Top: bias pot at B, middle: bias pot at D, bottom: bias pot at C).

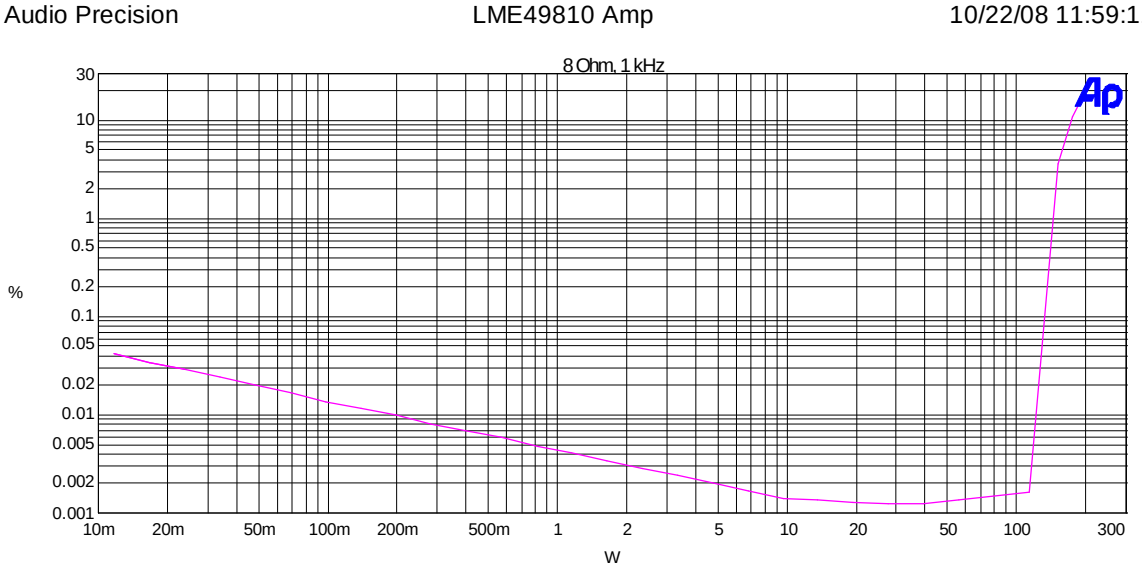

Figure 13 THD+N versus output level for 1 kHz, 8 Ω.

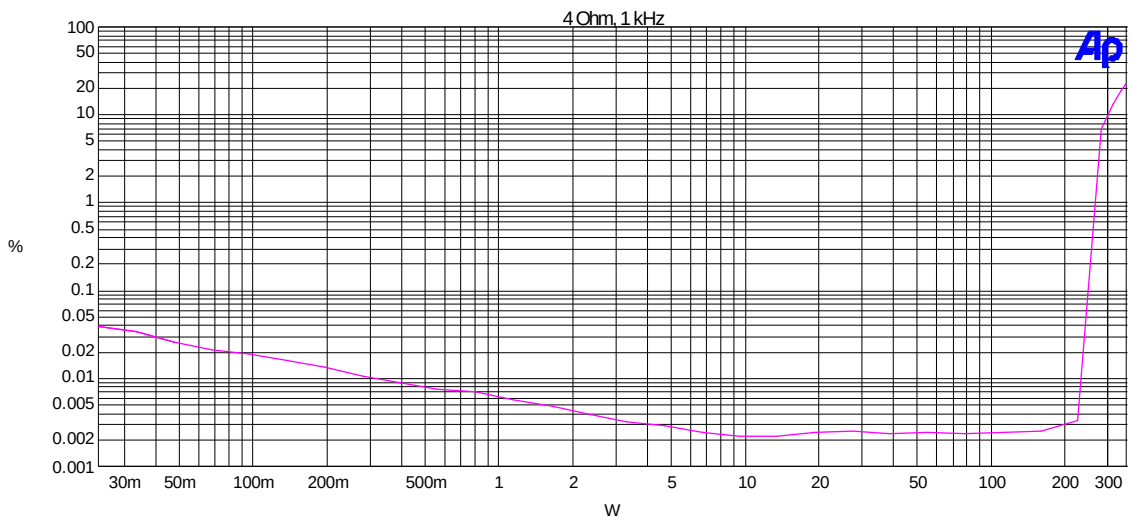

Figure 14 THD+N versus output level for 1 kHz, 4 Ω.

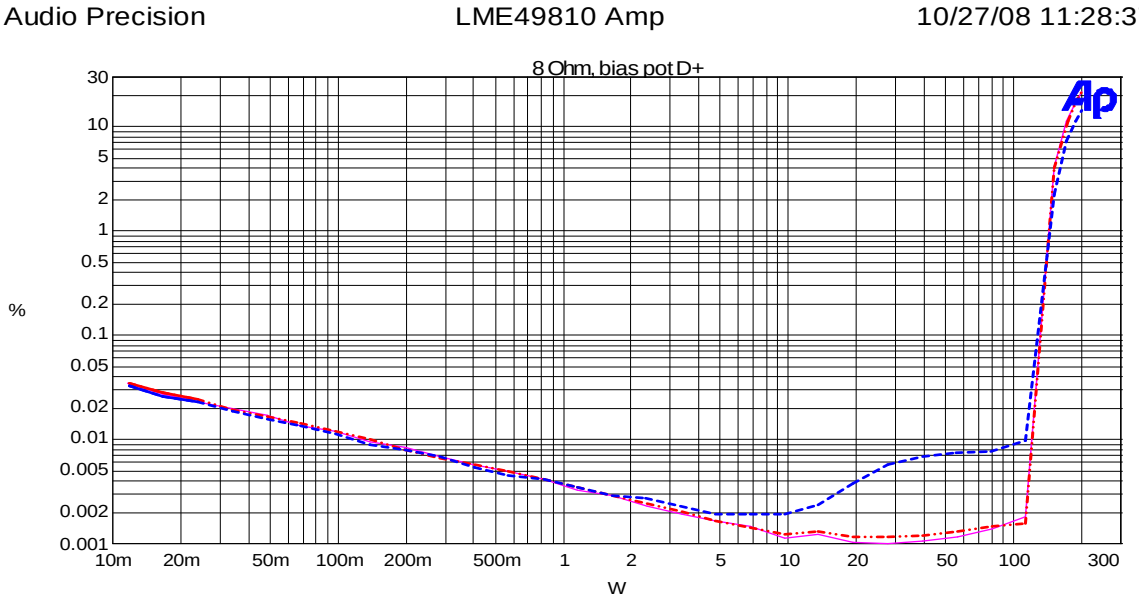

Figure 15 THD+N vs output level for 10 kHz, 1 kHz and 100 Hz (from top to bottom).

Performance Evaluation

THD+N versus output level of the amplifier for 8 Ω and 4 Ω load were measured. The measurement bandwidth is 22 Hz to 30 kHz. A 1 kHz signal was fed to the amplifier. From Figure 13 and 14, we observe that the 1% THD+N point for 8 Ω and 4 Ω are over 120 W and 240 W, respectively. The amplifier fully meets our expected output levels. When driving 4 Ω, the distortion slightly increased. THD+N versus output level for 100 Hz, 1 kHz and 10 kHz signals are shown in Figure 15.

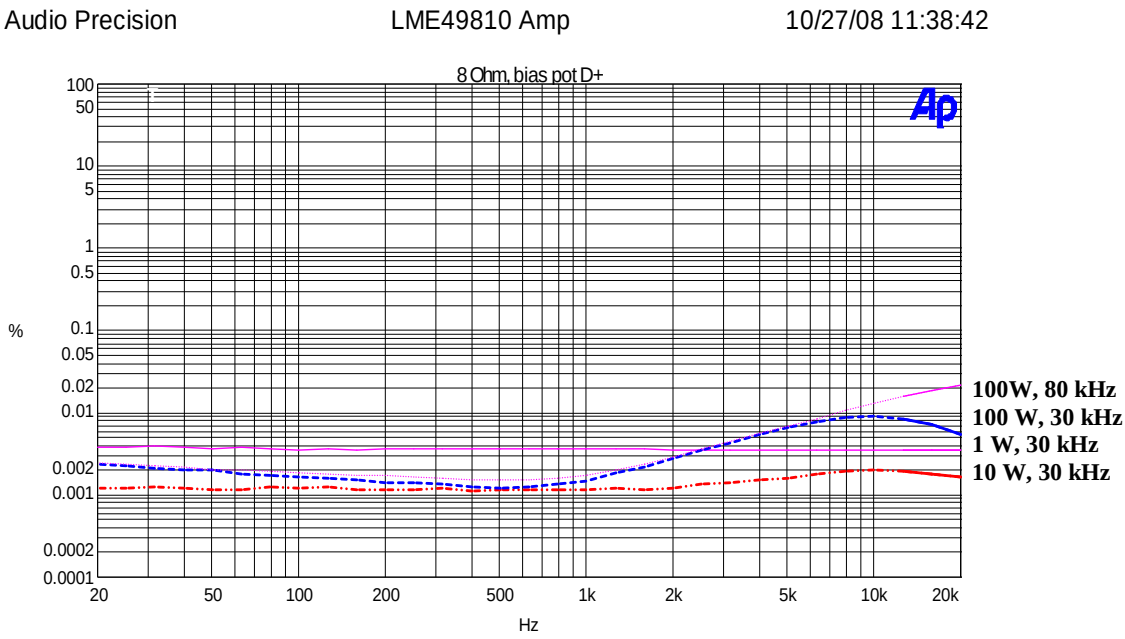

Figure 16 THD+N versus frequency for different output level (solid: 1 W, 30 kHz; dot-dash: 10 W, 30 kHz; dash: 100 W, 30 kHz; dot: 100 W, 80 kHz)

THD+N across the audio spectrum was measured next. Output level at 1 W, 10 W and 100 W are observed. We can see from Figure 16 that distortion increases gradually as frequency increased. This is a typical trend in most amplifiers with negative feedback. The amount of feedback reduces as a consequence of open-loop gain reduction as frequency going up. The overall amplifier achieves very low distortion across the whole audio spectrum.

Conventional THD+N analysis is a powerful tool to evaluate amplifier linearity. However, it does not offer accurate measurement for frequencies higher than 10 kHz. In practice, distortion analyzer considers harmonic contents falling within the measurement bandwidth. If a bandwidth of 22 Hz to 30 kHz is selected, the analyzer only measures up to third harmonics of a 10 kHz signal. We can increase the bandwidth to allow more harmonics to be considered. However, it also increases noise power in the measurement. Amplifier harmonic distortion can not be measured precisely.

Methods using two sinusoidal signals feeding the amplifier simultaneously are commonly employed to evaluate amplifier's high-band linearity. Since the amplifier is practically non-linear, its output contains intermodulation distortion (IMD) of the two sinusoidal signals. In the following, we follow SMPTE and CCIF recommendation to perform IMD test. SMPTE specifies two frequencies: F_1 = 60 Hz and F_2 = 7 kHz. They are linearly combined where the high-frequency tone amplitude is ¼ that of the low-frequency tone. If there is IMD, they appear as a family of sidebands around the high-frequency tone ($F_2 \pm F_1$, $F_2 \pm 2F_1$, etc.). Figure 17 shows the 1 W output signal spectrum of SMPTE test. We can see that the 7 kHz tone is surrounded by the aforementioned sidebands. If the output power is increased to 90 W, the energy of sidebands increases substantially as illustrated in Figure 18. SMPTE IMD versus output is depicted in Figure 19.

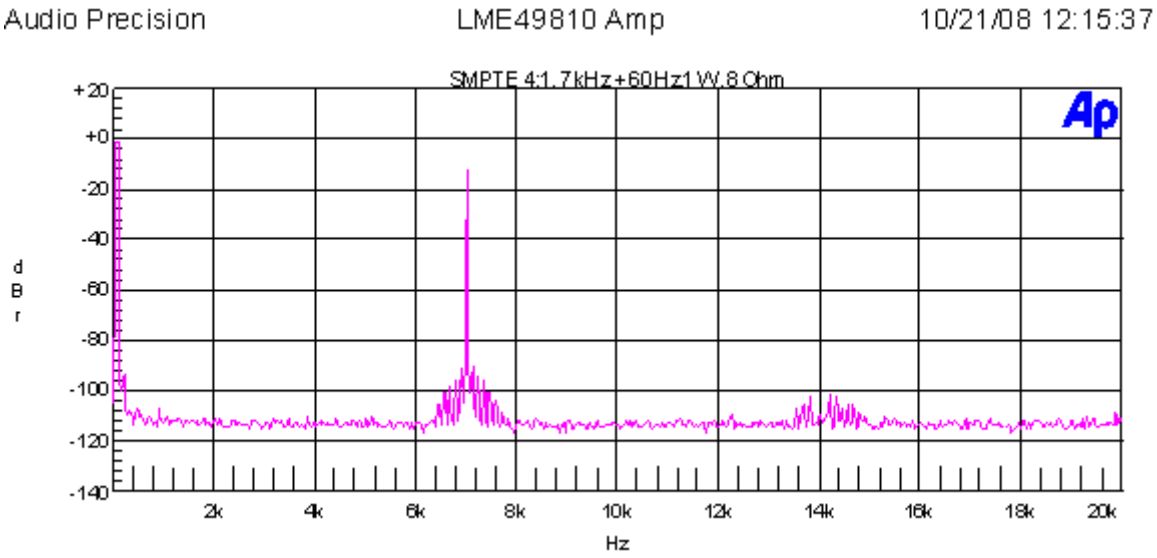

Figure 17 FFT of SMPTE output waveform at 1 W, 8 Ω.

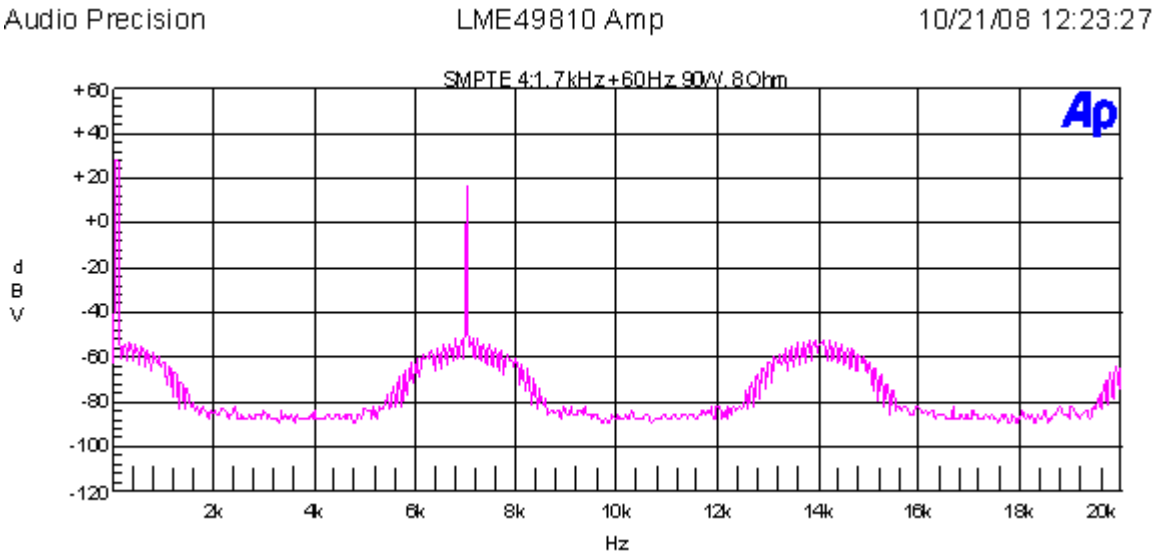

Figure 18FFT of SMPTE output waveform at 90 W, 8 Ω.

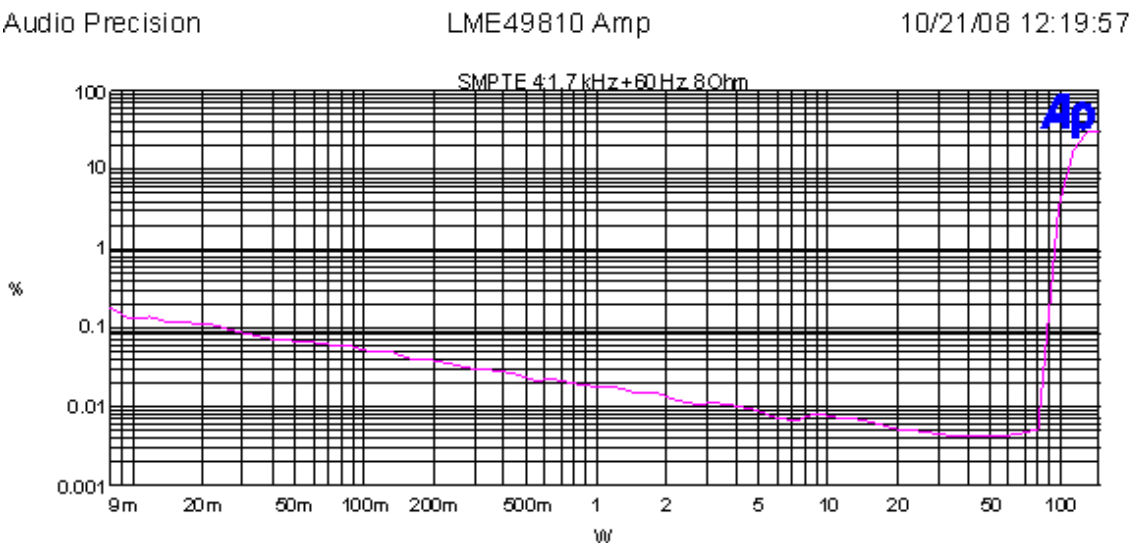

Figure 19 IMD vs output level for SMPTE test signal.

Two equal-amplitude high frequency tones (F_1 = 19 kHz and F_2 = 20 kHz) are used in CCIF IMD test. In this test, we only measure the low-frequency IMD product at $F_2 - F_1$ which is 1 kHz. Figure 20 shows the output signal spectrum for 19+20 kHz dual-tone test. The level of the 1 kHz harmonic is about 76 dB down compared to the test tones. The distortion level versus output power is plotted in Figure 21.

We also need to evaluate amplifier stability. The most direct approach is loop-gain measurement. However, it can also be evaluated by using square wave test. A 20 kHz square wave was fed to the amplifier. The output is shown in Figure 22. It can be seen that there is not ring at rising and falling edges. This implies that the amplifier is very stable.

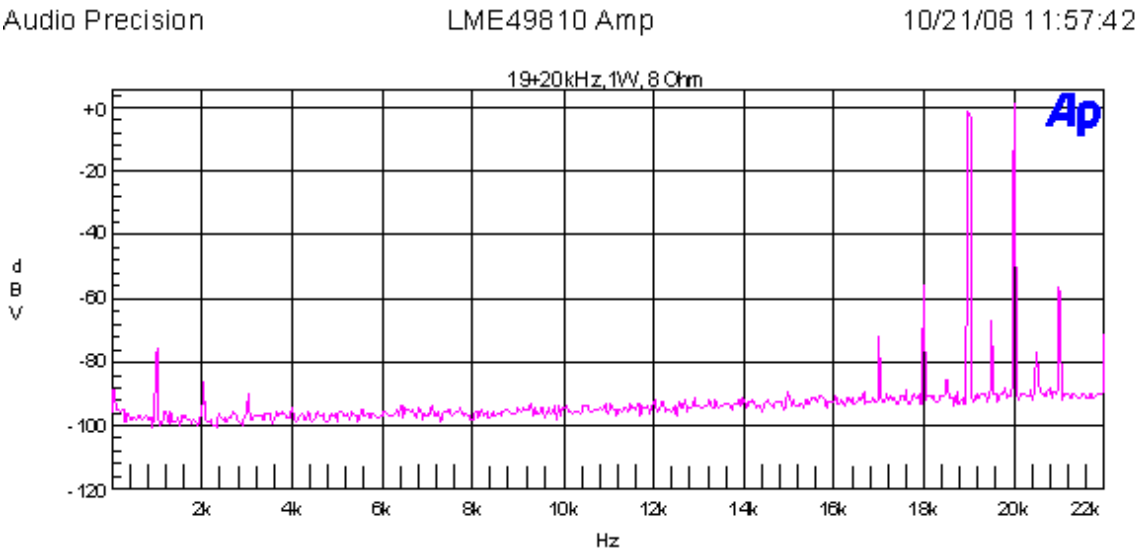

Figure 20 FFT of 19+20 kHz dual-tone waveform

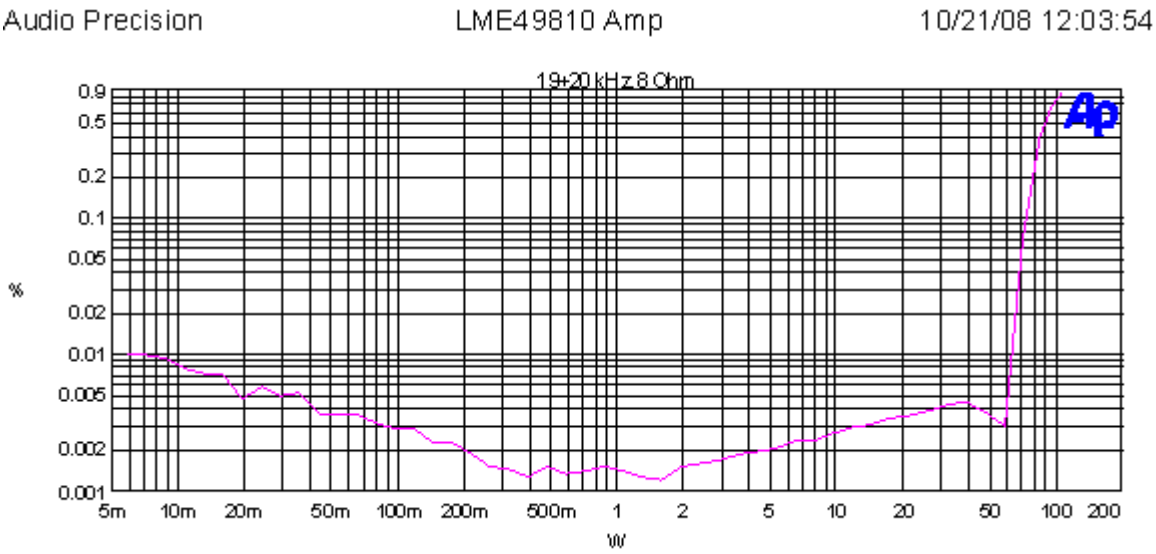

Figure 21 IMD vs output level for 19+20 kHz dual tone.

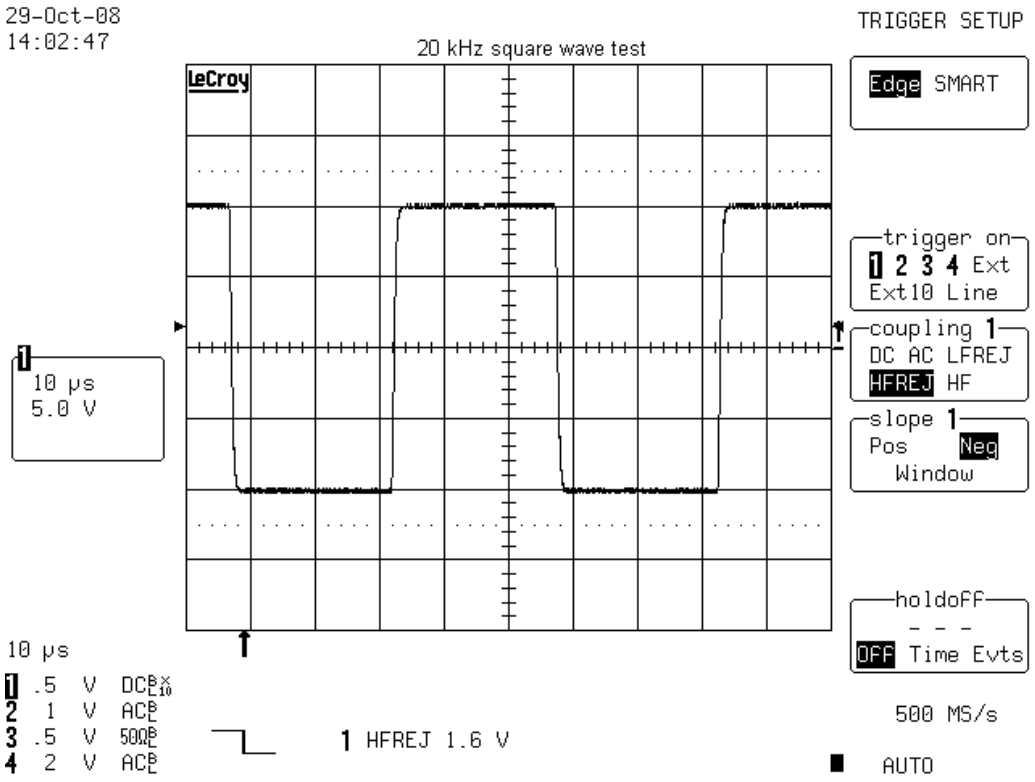

Figure 22 Square wave test to check amplifier stability.

